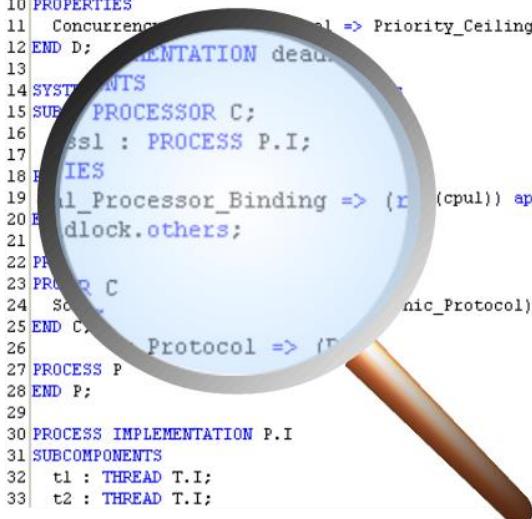


AADL Inspector 1.8

Quick Start Guide

```
5 SYSTEM AcquireLock;
6 END deadlock;
7
8 DATA D
9 -- deadlock occurs if concurrency control protocol is removed
10 PROPERTIES
11   Concurrency_Ceiling_Protocol => Priority_Ceiling_Protocol;
12 END D; IMPLEMENTATION deadlock;
13
14 SYSTEMS
15 SUBPROCESSOR C;
16   Ssl : PROCESS P.I;
17   FILES
18     Cpl_Processor_Binding => (r (cpul)) applies to process
20     deadlock.others;
21
22 PROCESSOR C
23   SoC <-
24   END C;
25   Protocol => (T)
26
27 PROCESS P
28 END P;
29
30 PROCESS IMPLEMENTATION P.I
31 SUBCOMPONENTS
32   t1 : THREAD T.I;
33   t2 : THREAD T.I;
```

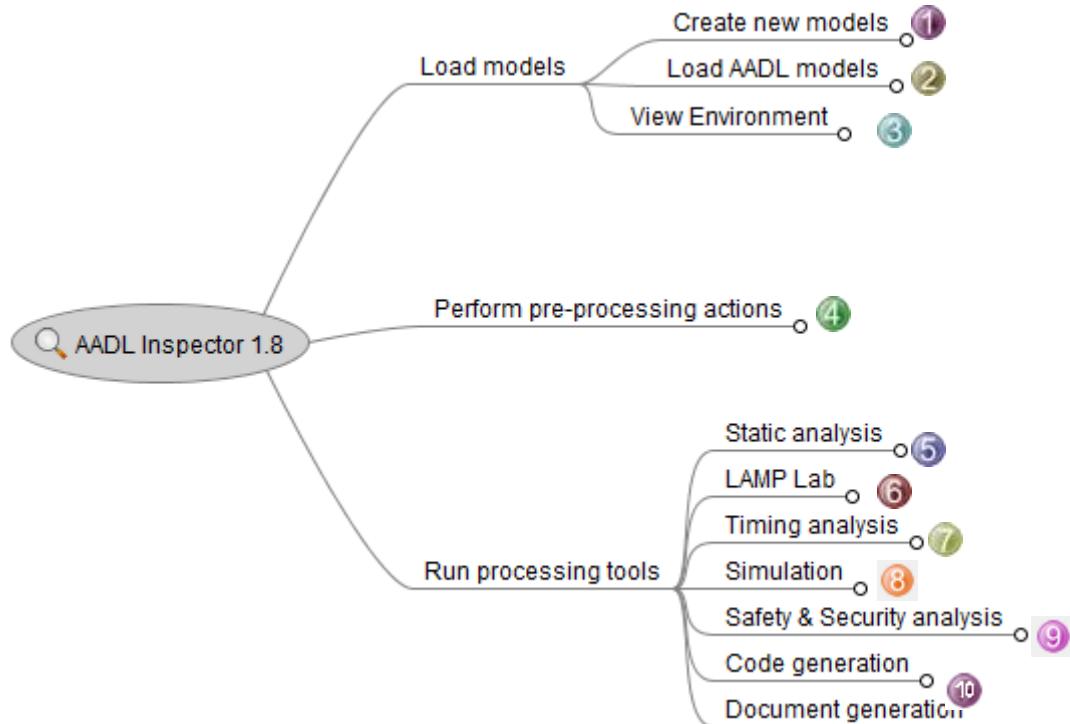


Overview

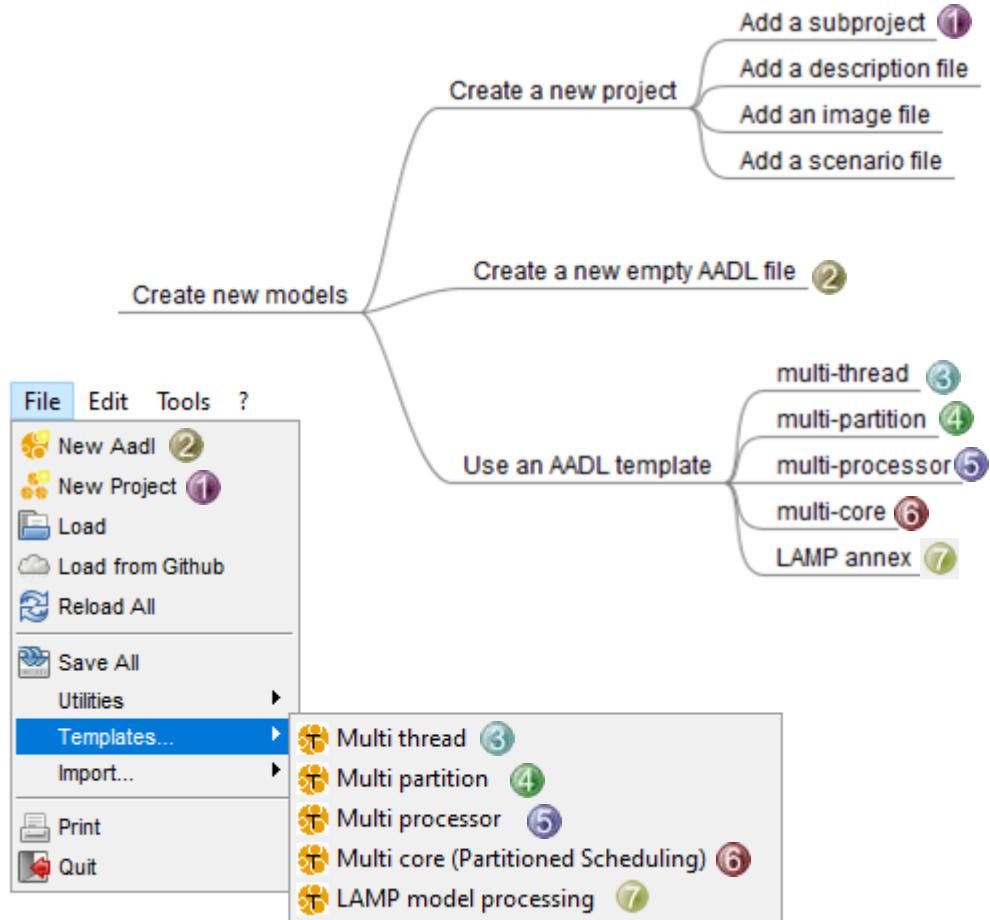
The image shows the AADL Inspector 1.8 interface with four main components:

- Project Browser**: On the left, it displays the project structure and files. A large blue arrow points from the text "Project Browser" down to the browser area.
- AADL Textual Editor**: In the center-left, it shows the AADL code for the control_system.aadl file. A large blue arrow points from the text "AADL Textual Editor" down to the editor area.
- Analysis Tools**: On the right, it shows various analysis results and tools. It includes a "Static Analysis" table and several performance monitoring charts (Deadline, Computed, Max Cheddar, Avg Marzil) for components like actuator.act_cpu, dashboard.dsdb_cpu, and network. A large blue arrow points from the text "Analysis Tools" down to the analysis area.
- Simulator**: At the bottom right, it shows a circular gauge with a red needle pointing towards 100, indicating system health or performance levels.

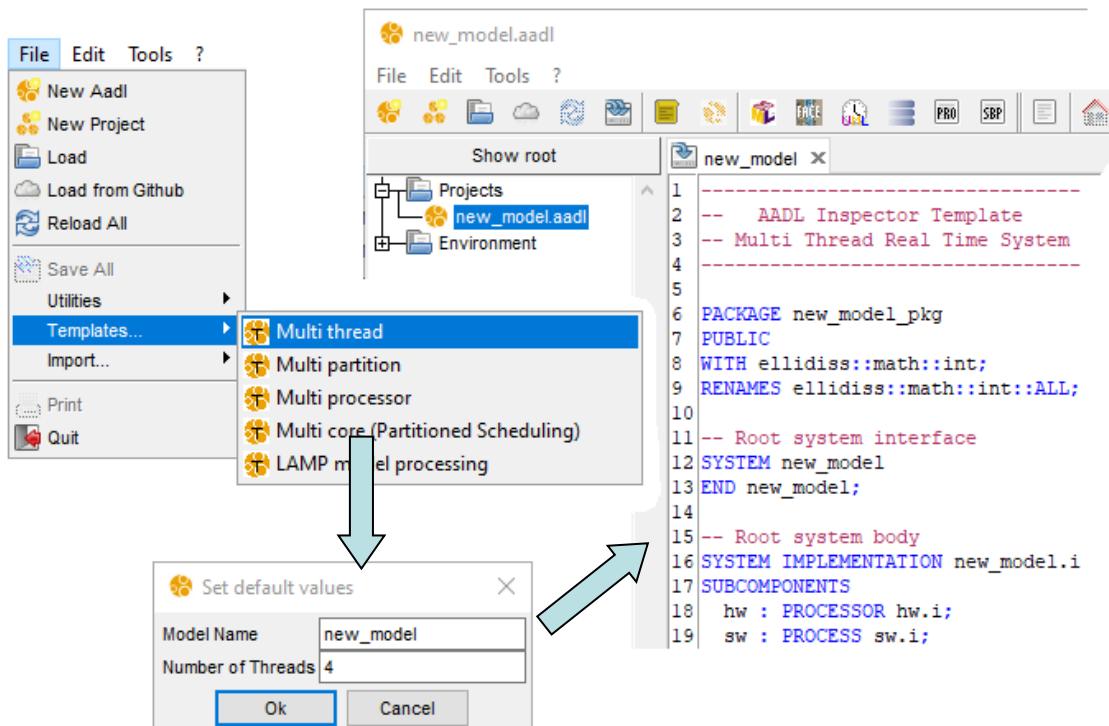
Overview



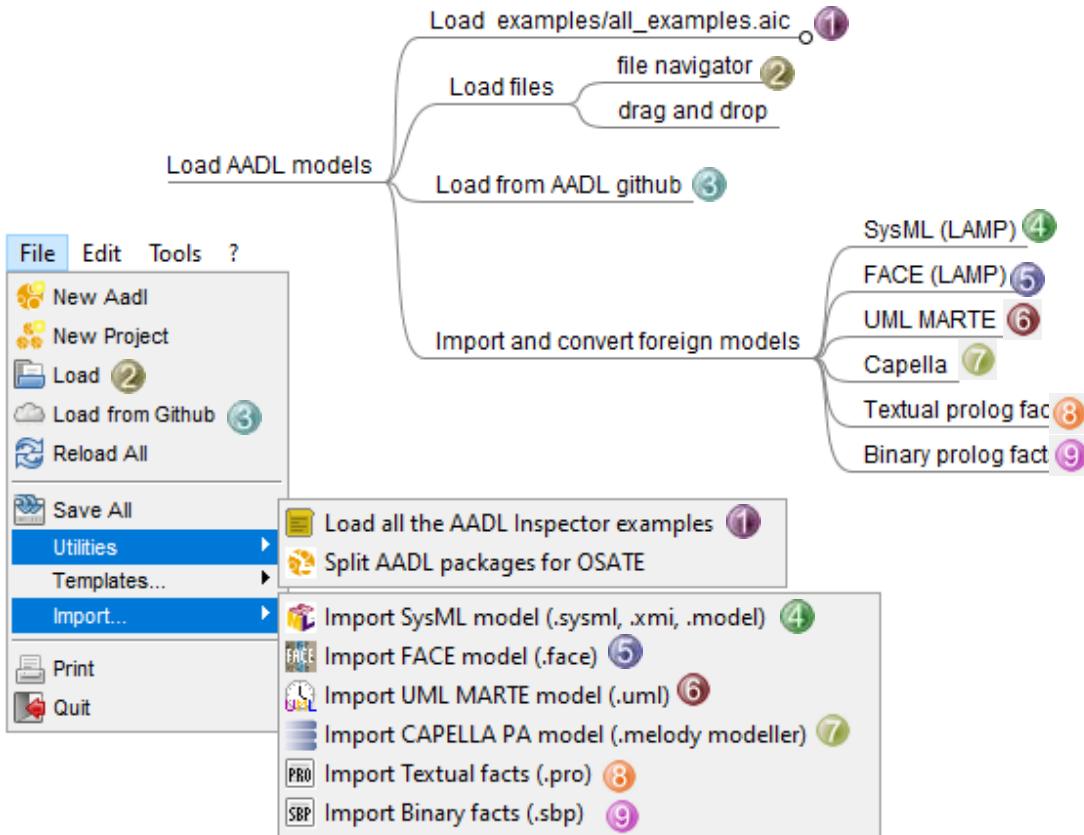
1. Create New Models



1. Create New Models example



2. Load Existing Models



2. Load Existing Models example

D:/Projetos/AADLInspector/AI-1.8/examples/readme.txt

File Edit Tools ?

Show root Description X

AADL INSPECTOR EXAMPLES

The examples are organized in projects (files with a .aic extension): Deploy the tree in the left hand side browser and select a project by clicking on the corresponding icon.

Elements can be individually selected or deselected by a simple click on its icon.

Only the files that have an icon with a green tick will be processed. The available processing tools are in the right hand side tabs:

- * static analysis: various predefined parsing and processing tools
- * lamp lab: custom analysis tools with LAMP annexes
- * timing analysis: schedulability analysis, simulation and flow latency
- * safety & security analysis: Fault Tree Analysis and Security Rules checker
- * code generation: interface to launch Ocicina back-ends
- * doc generation: quickly build an analysis report in PDF

Summary of proposed examples:

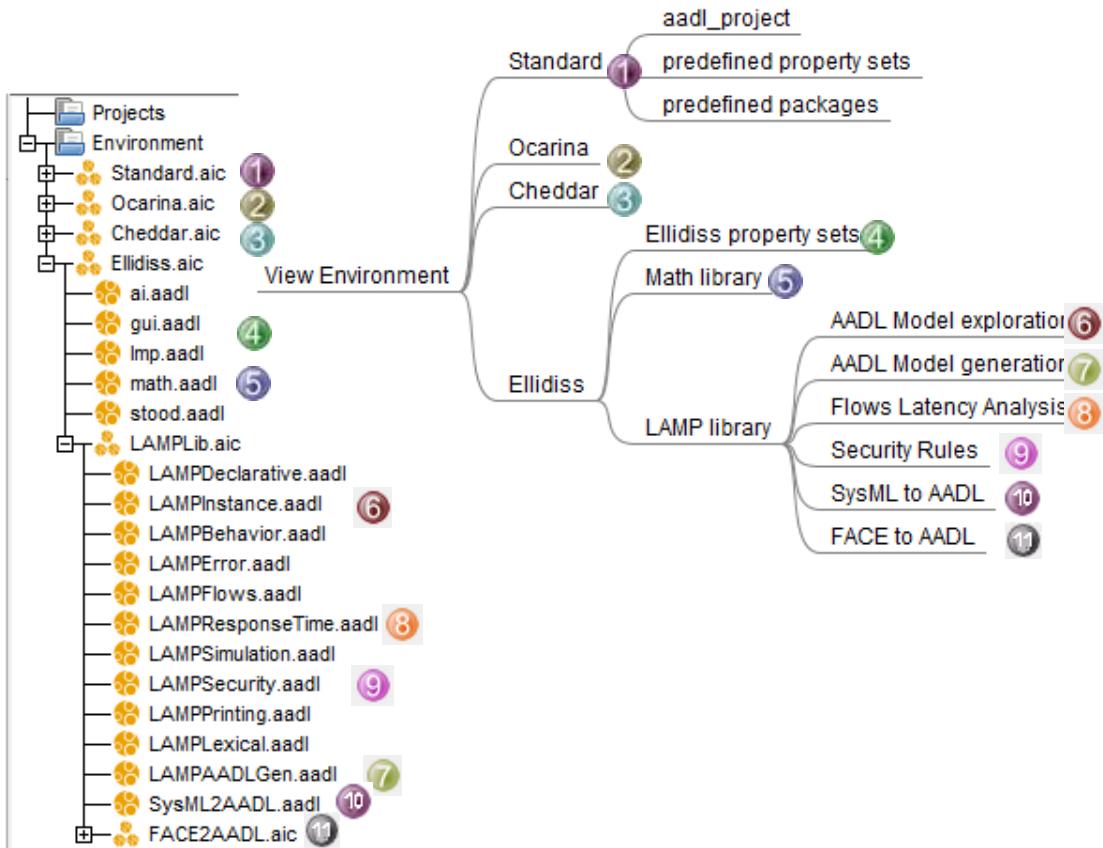
A: denotes use of AADL ARINC 653 Annex
B: denotes use of AADL Behavior Annex
C: denotes use of AADL Core 2.2 (SAE AS-5506C)
E: denotes use of AADL Error Modelling Annex (EMV2)
L: denotes use of AADL LAMP Annex (model processing language)
S: denotes use of simulation scenario (.asc files)

- patterns.aic:
Contains seven sub-projects listed below.
They illustrate the main communication and scheduling protocols that are supported by AADL and can be analysed with AADL Inspector.

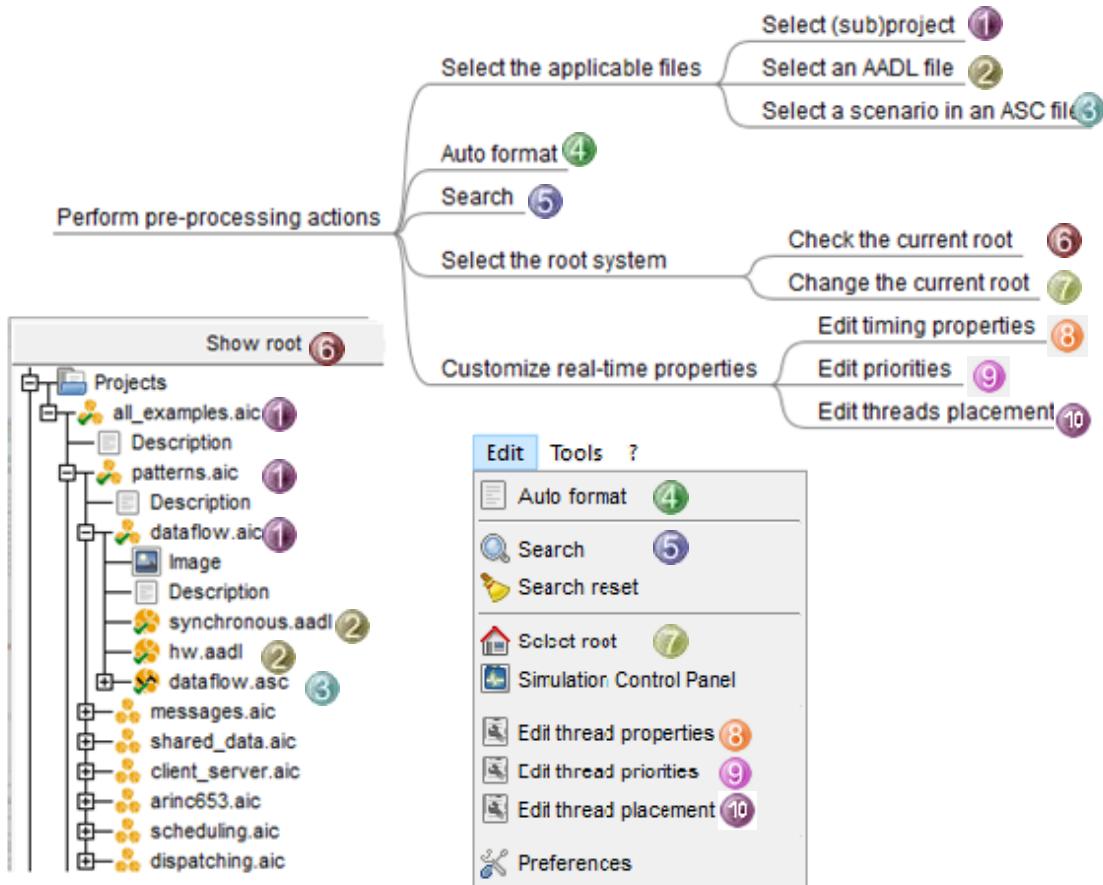
- dataflow.aic: [BCS]
Dataflow communication between threads.
It can be used to observe the effect of Sampled, Immediate and Delayed data port connections.

- messages.aic: [BC]

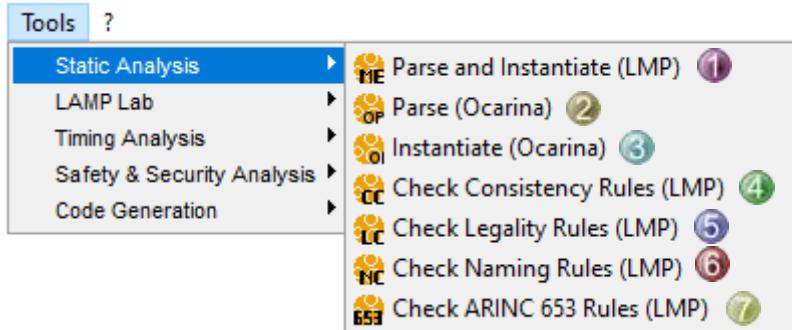
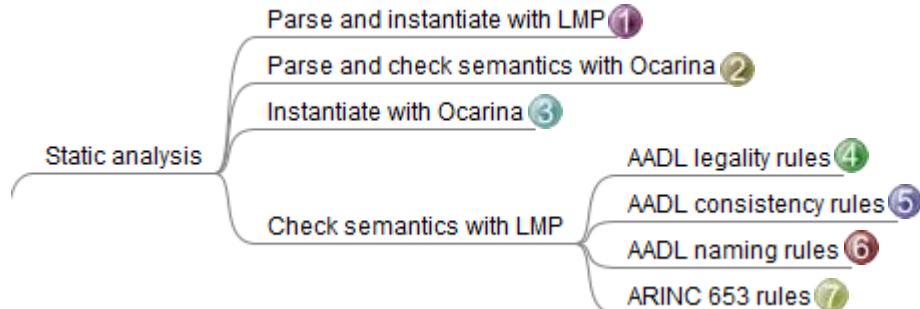
3. View environment



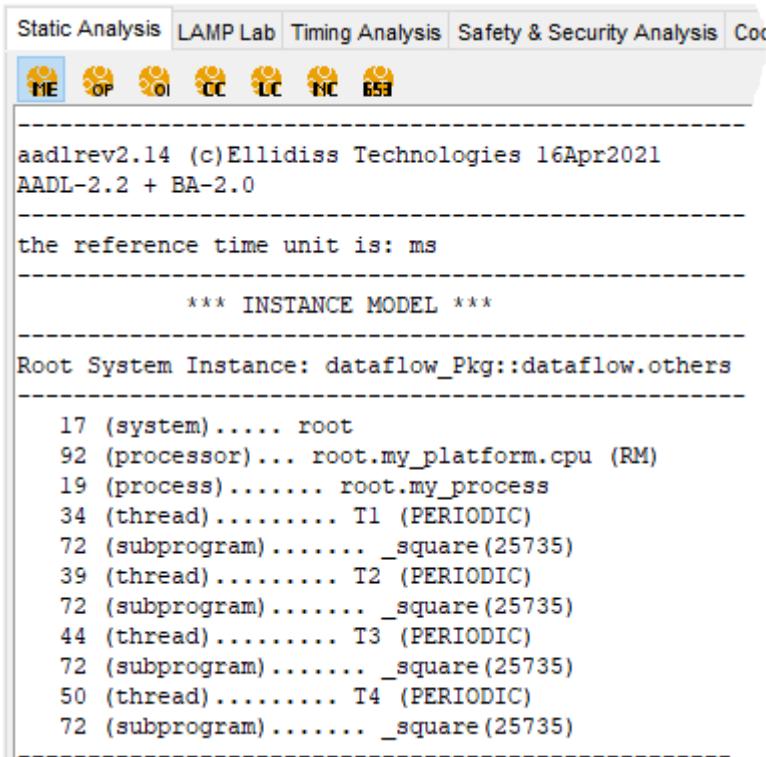
4. Pre-Processing



5. Static Analysis



5. Static Analysis example



The screenshot shows the AADL Inspector interface with the 'Static Analysis' tab selected. Below the tabs, there are icons for ME, OP, OI, CC, LC, NC, and ESS. The main window displays the following output:

```
aadlrev2.14 (c) Ellidiss Technologies 16Apr2021
AADL-2.2 + BA-2.0
-----
the reference time unit is: ms
-----
*** INSTANCE MODEL ***
-----
Root System Instance: dataflow_Pkg::dataflow.others
-----
17 (system)..... root
92 (processor).... root.my_platform.cpu (RM)
19 (process)..... root.my_process
34 (thread)..... T1 (PERIODIC)
72 (subprogram).... _square(25735)
39 (thread)..... T2 (PERIODIC)
72 (subprogram).... _square(25735)
44 (thread)..... T3 (PERIODIC)
72 (subprogram).... _square(25735)
50 (thread)..... T4 (PERIODIC)
72 (subprogram).... _square(25735)
```

6. LAMP Lab



LAMP Lab

- Execute
 - Run LAMP (1)
 - LAMP query (2)
- Add/Remove
 - Add raw XML/XMI facts (3)
 - Add SysML facts (4)
 - Add FACE facts (5)
 - Add simulation event facts (6)
 - Add response time facts (7)
 - Add native prolog code (8)
 - Clean up all add-ons (9)
- Show
 - Show LAMP console
 - Show AADL declarative model facts
 - Show AADL instance model facts
 - Show imported XML/XMI facts
 - Show imported SysML facts
 - Show imported FACE facts
 - Show imported simulation event facts
 - Show imported response time facts
 - Show imported prolog code

Tools ?

- Static Analysis >
- LAMP Lab (1)
- Timing Analysis
- Safety & Security Analysis
- Code Generation
- Run LAMP (1)
- LAMP query (2)
- Add raw XML/XMI facts (3)
- Add SysML facts (4)
- Add FACE facts (5)
- Add simulation events facts (6)
- Add response time facts (7)
- Add native prolog code (8)
- Clean up all add-ons (9)
- Show LAMP console
- Show AADL declarative model facts
- Show AADL instance model facts
- Show imported XML/XMI facts
- Show imported SysML facts
- Show imported FACE facts
- Show simulation event facts
- Show response time facts
- Show Imported prolog facts or rules

6. LAMP Lab example

Static Analysis LAMP Lab Timing Analysis Safety & Security Analysis Code Generation Doc Generation



```
/*****
 *          LAMP console
 * (c) Ellidiss Technologies, 2021
 \****/
```

[x] AADL facts base loaded.
[] no XML facts base loaded.
[] no SysML facts base loaded.
[] no FACE facts base loaded.
[x] Simulation facts base loaded.
[] no Response Time facts base loaded.
[] no Native Prolog facts base loaded.
[x] LAMP rules base loaded.
[x] LAMP queries loaded.

LAMP> execution started.

hello!
the reference time unit is: us
last simulation trace id: 20210507-094433

=====

Checking LAMPExample1_Pkg::s.i

=====

```
root.a : PROCESS LAMPExample1_Pkg::a.i
root.a.tl : THREAD LAMPExample1_Pkg::t
root.a.t2 : THREAD LAMPExample1_Pkg::t
root.a.t3 : THREAD LAMPExample1_Pkg::t
```

7. Timing Analysis

Timing analysis

- Thread response time and processor load with Cheddar and Marzin ①
- Static simulation over the hyper period with Cheddar ②
- Schedulability tests with Cheddar ③
- Schedulability simulation with Cheddar ④
- Scheduling Aware Flow Latency Analysis (LAMP) ⑤

Tools ?

Static Analysis ▶

LAMP Lab ▶

Timing Analysis ▶

Safety & Security Analysis ▶

Code Generation ▶

Processor Load & Thread Response Time Analysis ①

Simulation Timelines (Cheddar) ②

Theoretical Tests (Cheddar) ③

Simulation Tests (Cheddar) ④

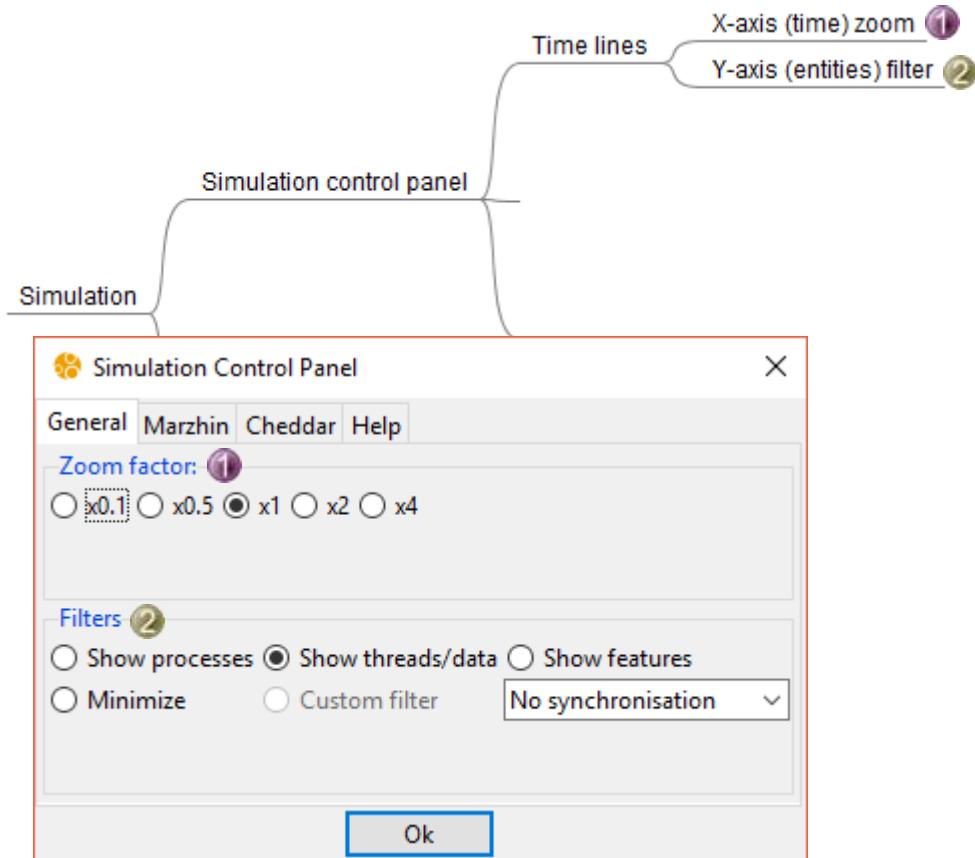
Scheduling Aware Flows Latency Analysis (SAFLA) with LAMP ⑤

<http://beru.univ-brest.fr/cheddar/>

7. Timing Analysis example

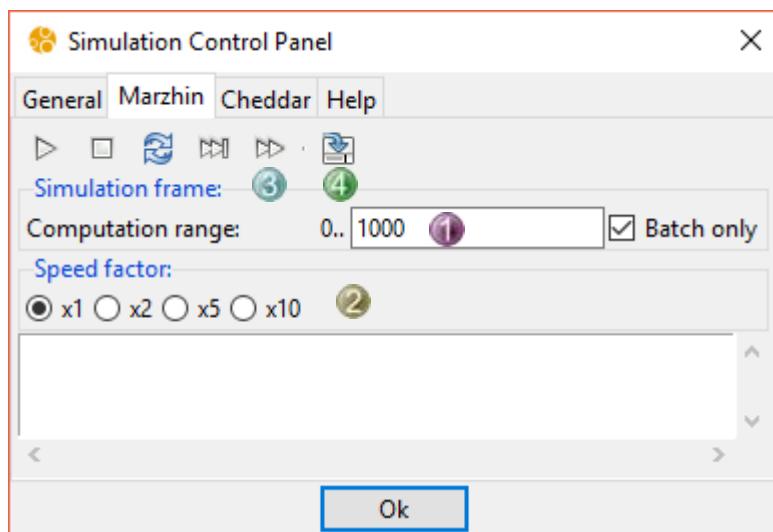
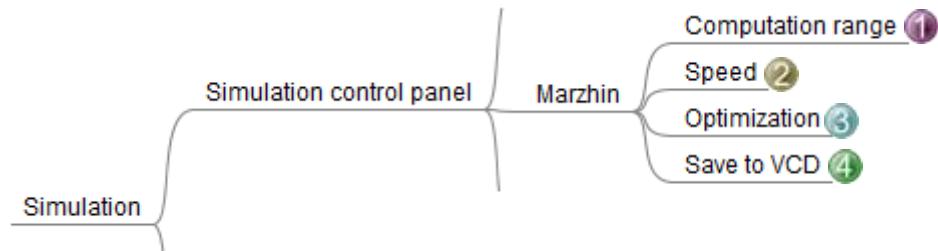
	Deadline	Computed	Max Cheddar	Max Marzhin	Avg Cheddar	Avg Marzhin	Min Cheddar	Min Marzhin
dashboard.dashboardcpu		30.00 %		31.40 %				
dashboard.dashboardsw								
elaboratecommand	20	4.00000	4	4	4.00	4.00	4	4
displaystatus	10	2.00000	2	2	2.00	2.00	2	2
motors.motorscpu		56.67 %		58.96 %				
motors.motorssw								
leftcontroller	15	7.00000	7	7	5.50	5.50	4	4
rightcontroller	15	5.00000	5	5	3.50	3.50	2	2
motorsmanager	10	3.00000	3	3	3.00	3.00	3	3
mainecu.maincpu		55.00 %		57.23 %				
mainecu.mainsw								
controlmanager	20	8.00000	8	8	8.00	8.00	8	8
statusmanager	10	3.00000	3	3	3.00	3.00	3	3
can		80.00 %		79.77 %				
VirtualLink								
cnx_0		2.00000	11	9	11.00	6.22	11	4
cnx_3		3.00000	9	10	9.00	4.65	9	3
cnx_4		3.00000	6	10	6.00	5.29	6	3
cnx_6		2.00000	13	5	13.00	3.11	13	2

8. Simulation timelines preferences



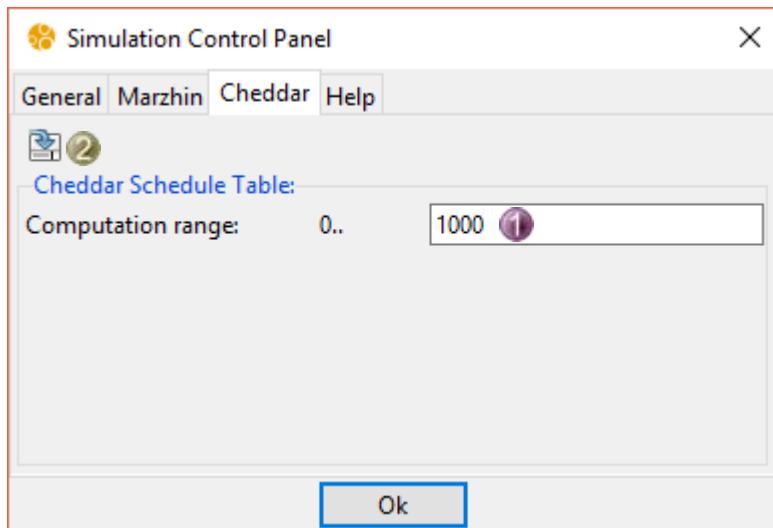
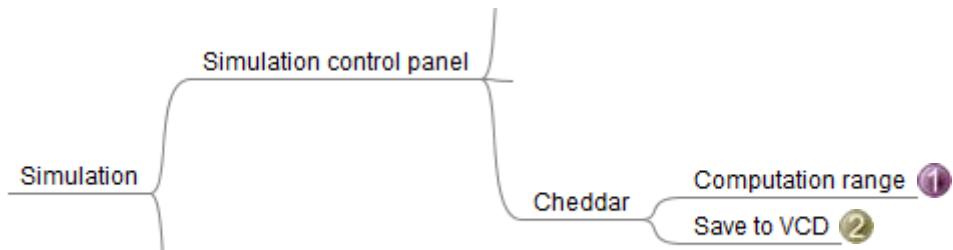
8. Simulation

Marzhin preferences

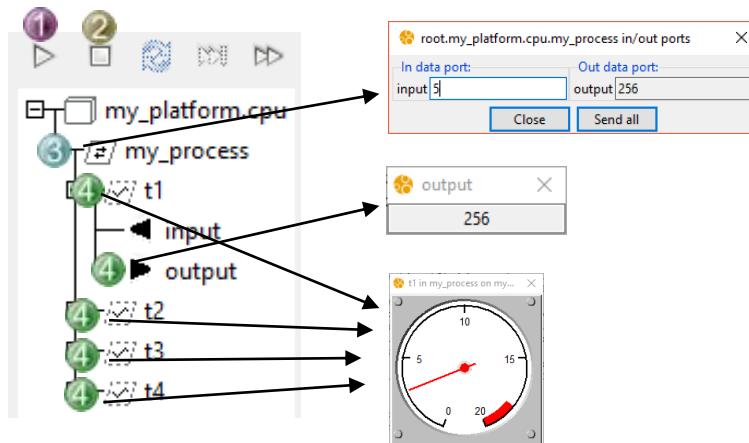
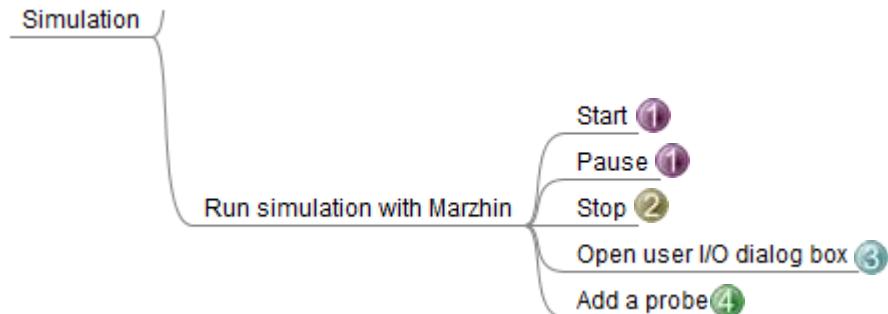


8. Simulation

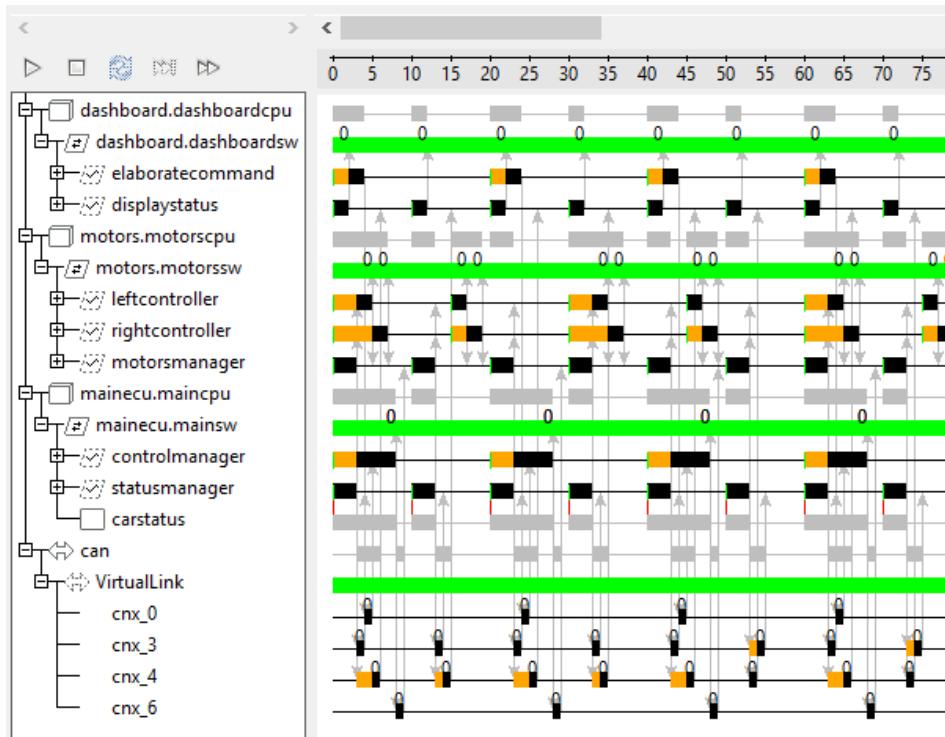
Cheddar preferences



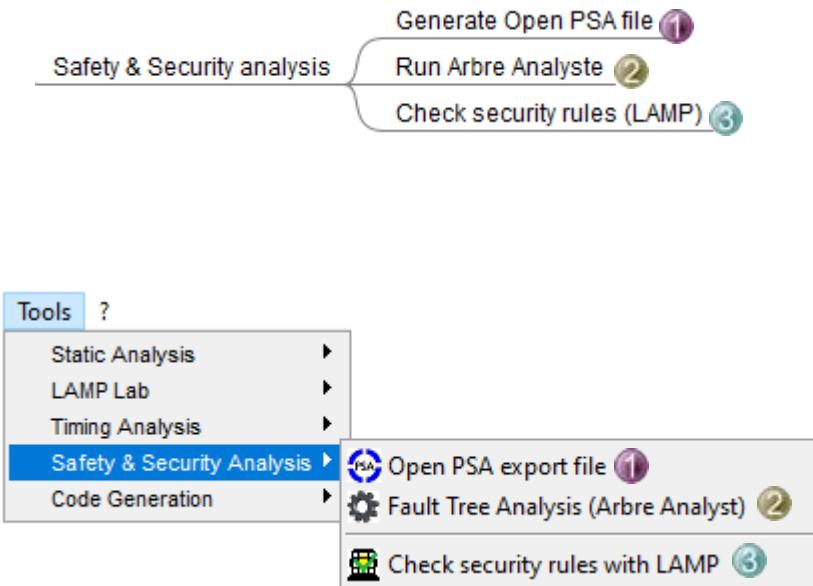
8. Simulation dashboard



8. Simulation example

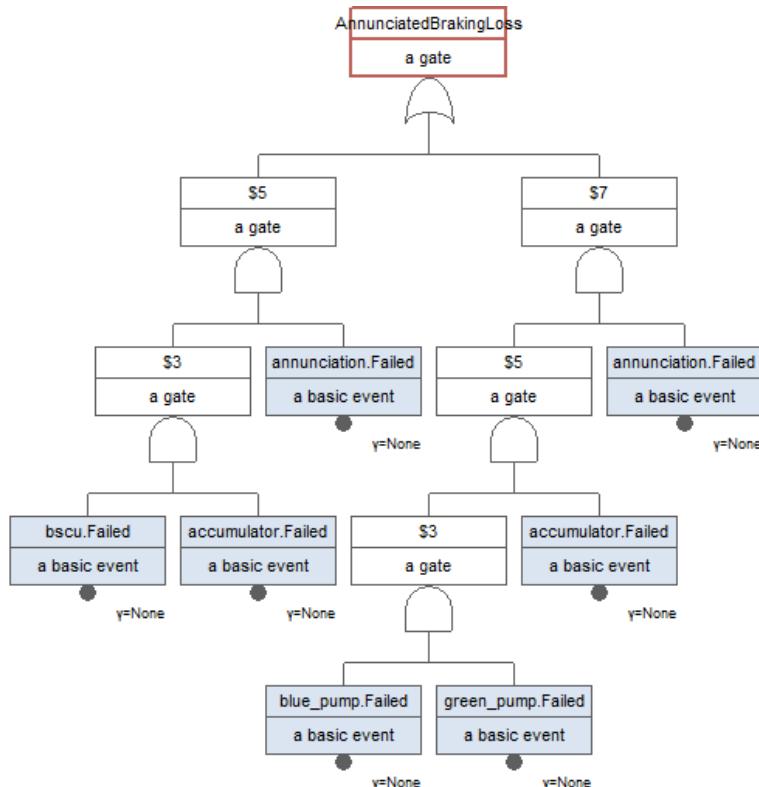


9. Safety & Security Analysis



9. Safety & Security Analysis

Fault Tree Analysis

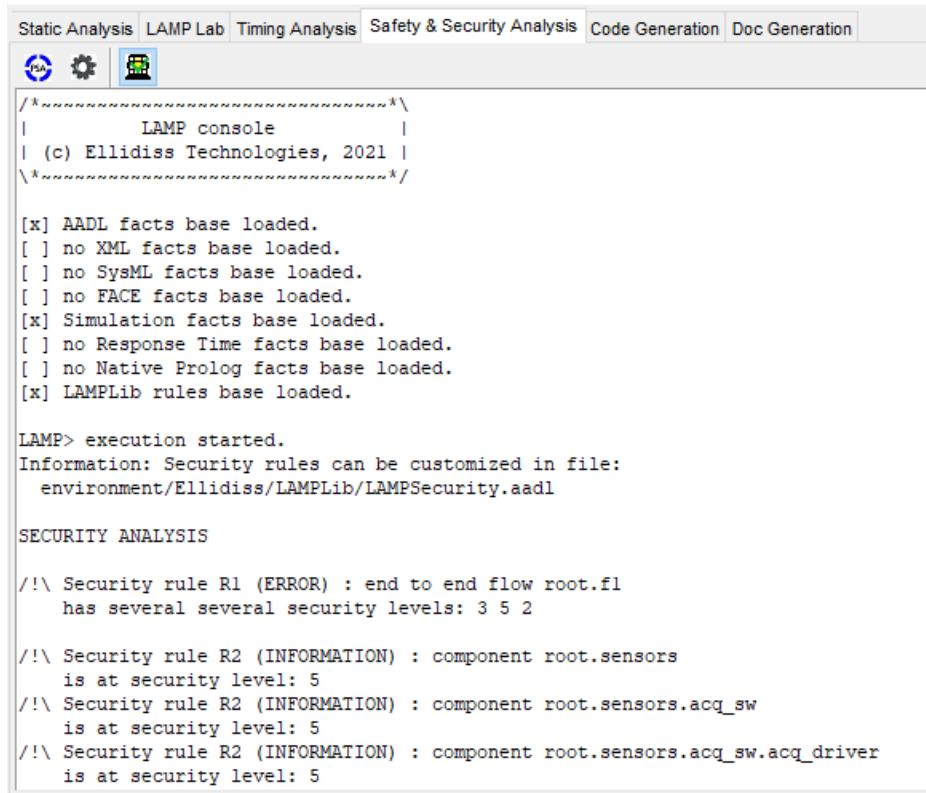


<https://www.arbre-analyste.fr/en.html>

9. Safety & Security Analysis

Security Rules

Static Analysis LAMP Lab Timing Analysis Safety & Security Analysis Code Generation Doc Generation



```
/*-----*\\
|          LAMP console           |
| (c) Ellidiss Technologies, 2021 |
\\-----*/
```

```
[x] AADL facts base loaded.
[ ] no XML facts base loaded.
[ ] no SysML facts base loaded.
[ ] no FACE facts base loaded.
[x] Simulation facts base loaded.
[ ] no Response Time facts base loaded.
[ ] no Native Prolog facts base loaded.
[x] LAMPLib rules base loaded.

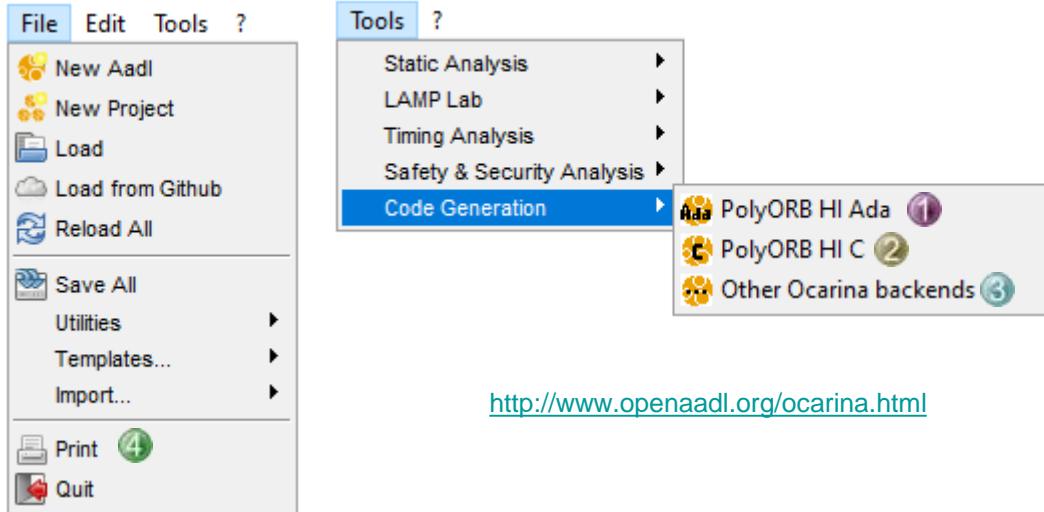
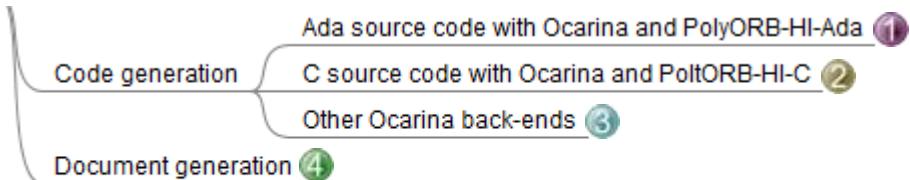
LAMP> execution started.
Information: Security rules can be customized in file:
environment/Ellidiss/LAMPLib/LAMPSecurity.aadl

SECURITY ANALYSIS

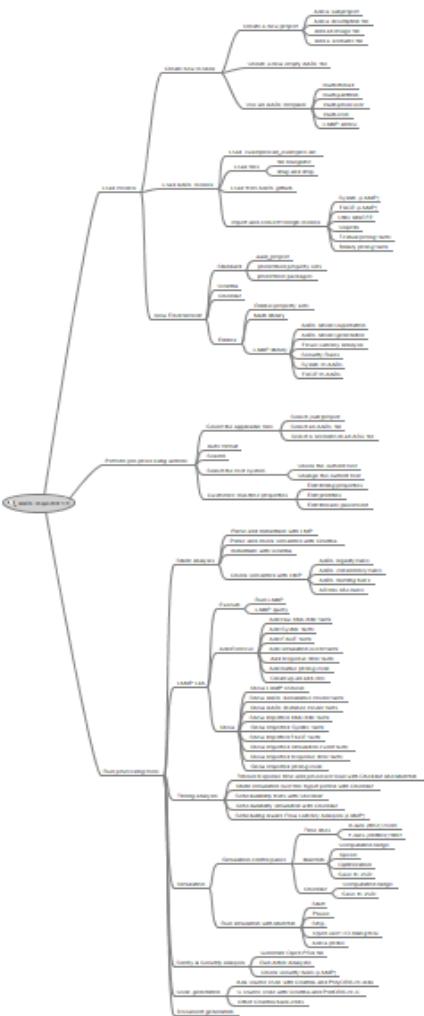
//\ Security rule R1 (ERROR) : end to end flow root.fl
    has several several security levels: 3 5 2

//\ Security rule R2 (INFORMATION) : component root.sensors
    is at security level: 5
//\ Security rule R2 (INFORMATION) : component root.sensors.acq_sw
    is at security level: 5
//\ Security rule R2 (INFORMATION) : component root.sensors.acq_sw.acq_driver
    is at security level: 5
```

10. Code & Document Generation



More Information



Help
About
License info

Open install dir
Open config dir
Open tmp dir
Open doc dir
Open code dir

- [AADL Inspector 1.8 Quick Start](#)
- [**AI User Manual**](#)
- [Cheddar](#)
- [Consistency Rules](#)
- [Legality Rules](#)
- [Marzhin](#)
- [Metrics](#)
- [Naming Rules](#)
- [ocarina](#)
- [polyorb-hi-ada_ug](#)
- [polyorb-hi-c_ug](#)

<http://www.ellidiss.com>

aadl@ellidiss.com