



AADL Inspector

Model processing framework for the
Architecture Analysis and Design Language

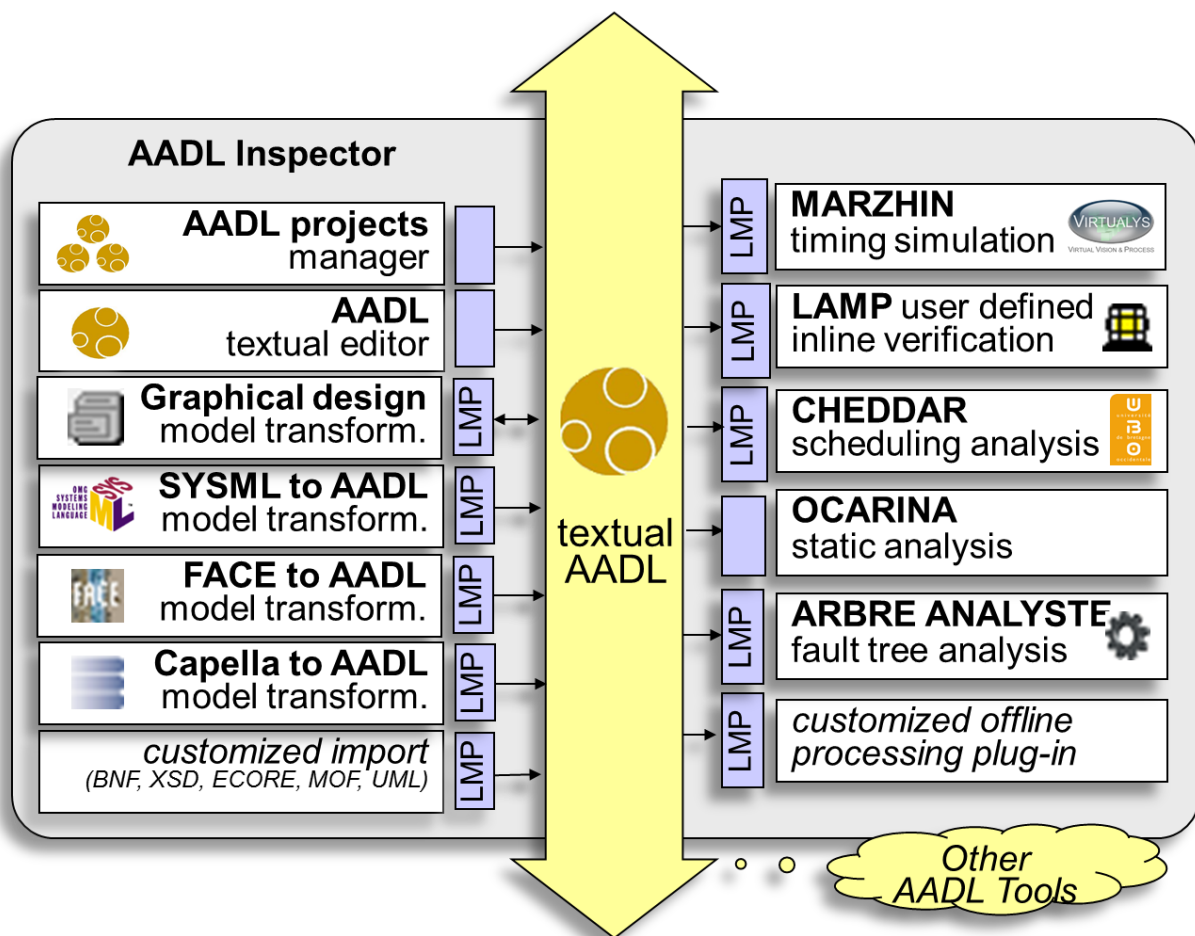
```
5 SYSTEM deadlock
6 END deadlock;
7
8 DATA D
9 -- deadlock occurs if concurrency control protocol is removed
10 PROPERTIES
11   Concurrency_Control_Protocol => Priority_Ceiling_Protocol;
12 END D;
13
14 SYSTEM IMPLEMENTATION deadlock
15 SUBCOMPONENTS
16   cpu : PROCESSOR C;
17   process1 : PROCESS P.I;
18 PROPERTIES
19   Actual_Processor_Binding => (cpu) applies to process1;
20 END deadlock.others;
21
22 PROCESSOR C
23 PROPERTIES
24   Scheduler_Protocol => (Priority_Ceiling_Protocol);
25 END C;
26
27 PROCESS P
28 END P;
29
30 PROCESS IMPLEMENTATION P.I
31 SUBCOMPONENTS
32   t1 : THREAD T.I;
33   t2 : THREAD T.I;
```

Real-Time



AADL: designing scalable safe and secure real-time systems.

Modeling and early validation of software architectures is a key concern for embedded applications. The Architecture Analysis and Design Language (AADL) is a textual and graphical language dedicated to design and analysis of architectural models of applicative software and its execution platform. AADL Inspector can process AADL v2.3 (SAE AS-5506D) as well as its Behavior Annex and Error Annex extensions. The rich semantics of AADL enable the specification of advanced assurance cases sharing a common representation of the system and involving a variety of analysis domains including static properties, real-time, safety and security. Thanks to its textual syntax, AADL is scalable and can be used as a first-class front end modelling language for designing large scale software intensive systems or as a pivot format to implement software development toolchains.



Toolchain integration:

Thanks to the AADL textual notation, AADL Inspector can easily be integrated into heterogeneous development toolchains. AADL textual specifications can be produced by AADL graphical editors such as Stood for AADL, by Domain Specific Language editors or even by a basic text editor. In addition, AADL source code can be automatically generated by model transformations of system engineering modeling sources such as FACE™, SysML or Capella. A direct access to AADL model libraries that are available on GitHub is also provided. Additionally, the outcomes of the analysis tools are saved in XML, VCD (Value Change Dump) or Prolog formats for further processing.

AADL Inspector main features:

AADL Inspector is a light and standalone tool with an easy-to-use graphical user interface composed of three main parts:

- An AADL source file browser that allows for the definition of hierarchical projects and clear access to available libraries.
- A multi-files AADL text editor.
- A set of customizable tabs to activate and display the outcomes of processing tools.

The screenshot shows the AADL Inspector interface with several callout boxes pointing to specific features:

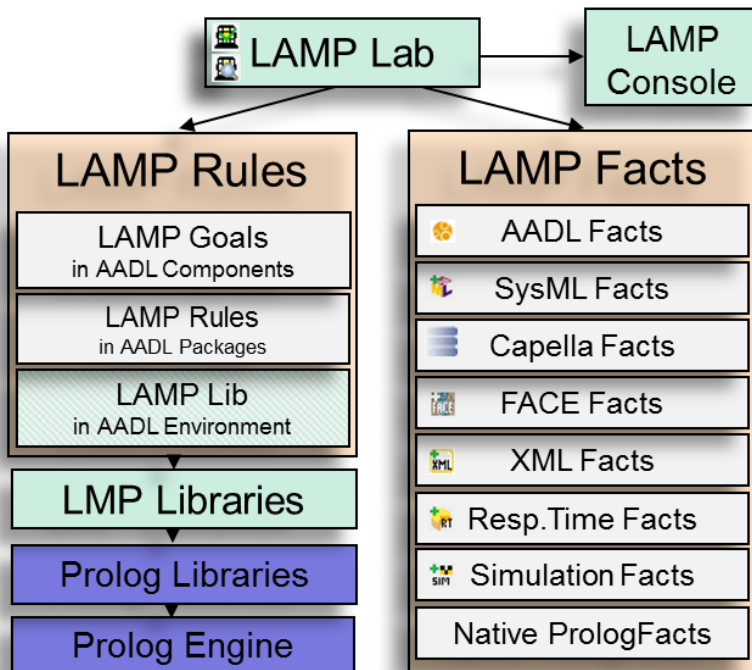
- Projects manager:** Points to the left sidebar showing a tree view of projects like 'at_examples.aic', 'calculator.aic', etc.
- LAMP: Flow analysis, Security analysis, Assurance cases:** Points to the top menu bar.
- Scheduling Analysis (Cheddar):** Points to the 'Scheduling Analysis' tab.
- Safety & Security analysis:** Points to the 'Security Analysis' tab.
- Model import: SysML, FACE, Capella/PA, ...:** Points to the 'Model' menu.
- Instance model export to graphical editor (Stood for AADL):** Points to the 'Export' menu.
- Response Time & CPU load:** Points to the 'Response Time' and 'CPU Load' tabs.
- Simulation (Marzhin):** Points to the 'Simulation' tab.
- Simulation I/O:** Points to the 'Simulation I/O' window showing a timeline and a gauge.

Processing tools included in AADL Inspector 1.8

- Import/Export tools:
 - o SysML to AADL (*LAMP*)
 - o FACE to AADL (*LAMP*)
 - o Capella PA to AADL (*LAMP*)
 - o AADL to HOOD (*LAMP*)
- Static analysis:
 - o AADL syntactic analysis (*LMP & Ocarina*)
 - o AADL legality rules (*LMP & Ocarina*)
 - o AADL instantiation (*LMP & Ocarina*)
- Timing analysis:
 - o Scheduling analysis (*Cheddar*)
 - o Static simulation over the hyper-period (*Cheddar*)
 - o Event-based simulation (*Marzhin*)
 - o Scheduling Aware Flow Latency Analysis (*LAMP*)
- Safety analysis
 - o Fault tree analysis (*Arbre Analyste*)
- Security analysis
 - o Security rules checker (*LAMP*)

Customized processing rules:

The LAMP Laboratory included in AADL Inspector 1.9 is a powerful tool that enables the specification of customized processing rules and the implementation of complex assurance cases. LAMP stands for Logical AADL Model Processing and consists in giving access to standard Prolog programs inside AADL annex subclauses associated with AADL packages and components. Ellidiss Technologies provides a set of tools to parse AADL and XML/XMI based languages as well as Prolog libraries containing model accessors and utilities to help the user to develop his own exploration, constraints, transformation, and architectural reasoning rules. Use of an existing standard formal and declarative language such as Prolog brings almost unlimited model processing possibilities.



SysML to AADL:

Most of existing SysML to AADL transformation tools are based on the definition of a dedicated UML profile to represent AADL constructs. This approach seems natural; however, it forces the system engineer to “think” AADL and requires SysML tool specific customizations.

On the contrary, our solution takes plain SysML XMI input files and applies LAMP transformation rules to build an AADL model. Source code of the transformation template is provided and can be customized to fit corporate or project specific SysML to AADL mapping.

A similar approach can be applied to any other model transformation.

Requirements:

- AADL Inspector runs as a standalone executable on PC Windows and Linux.
- A recent Java Run-time Environment (1.8 or more) is required to run the Marzhin simulator.
- End-user licenses can be issued for commercial, academic or evaluation purposes.
- Less than 80 Mb free disk space is needed to install the product.



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*Cheddar is developed by the University of Brest
Ocarina is developed by Telecom ParisTech, ISAE and ESA
Marzhin is developed by Ellidiss Technologies and Virtualys
Arbre Analyste is developed by Emmanuel Clément
FACE is a trademark of the Open Group*

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